HF-VHF SDR S/H Sample and Hold Receivers DR2H+ and DR2H++ From 30 KHz to 72(110) MHz - Make Them Simple as Possible With Outstanding Performances

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I read carefully discussion and comments about my SDR designs (especially at Russian SDR forum http://forum.cqham.ru). The biggest problems are related to the LO generating. My best SDR receivers are DR2A+ and DR2A++. They have a big disadvantage that local oscillator have to go 4 times higher than receiving frequency is. With latest technology SMT ICs 74LVC series limited useful bandwidth goes to 52MHz. I designed SMT SDR RX DR2G with useful bandwidth limited to the 110MHz. This design is based on use XOR gates for obtaining 90 degree LO shift necessary for I/Q SDR receiver. This solution has a weakness that correct work is highly dependable from LO shape. Ideal solution is that LO has 50-50 duty ratio what is hard to achieve. Many homebrew built DDS LO with easy to get and easy soldered AD9851 and useful bandwidth with my previously published designs was limited to 15-17MHz. I am presenting new S/H SDR receiver with very similar RF specifications as DR2A+ and DR2A++ have but with LO which is twice higher that receiving frequency is. Now receiving bandwidth is increasing to 72 MHz with AC ICs in DIL case or to the 110MHz with 74LVC ICs. Image rejection is very similar to the classic designs with Johnson counter in previously published designs especially if we have high pure sinusoidal LO drive. DR2H+ specifications are:

1. Receiving range is going from 30 kHz to 72 MHz for DIL ICs version!!! With built in last modern technology components like 74LVC74 and 74LVC4066 are and with external LO to 110MHz!!
2. IIP3 32-35dBm and it depends from setting and used programs. MDS -116 to -122dBm also with 24 bit external USB SB card Audigy NX2
3. Receiver image rejection is from 65 -30 dB with hardware realization only
4. Sensitivity 0.18-0.27uV for 10 dB S/N ratio, max S/N ratio I measured was 70dB.
5. SFDR (Spurious free dynamic range) is 93-94 dB, this results are with signals spaced 5 kHz and more. Results are not changing very much if we spaced two signals to classical 20 kHz or more (with new modern SMT ICs 74LVC4066 SFRD is 95-97dB).
6. RX 1 dB compression point is + 1dBm!!!
7. Receiver has built in 4 channel CMOS oscillator

I left possibility to build in some kind of input filter LP or BP type if we want to achieve max specifications and stop odd harmonic receiving especially. Practically experience is that harmonic receiving is reduced. The results of measuring are lower RX sensitivity around -35 to -10 dB for third harmonic than fundamental is. These results are not looking so good but my practical experience is that even with my big antenna like 84m delta loop is harmonic receiving isn’t problem for most HF bands. In the evening hours I can notice only weak presents of strong carriers from 7 MHz broadcast band during receiving weak HAM signals at 1.8MHz. Different samples of DIL D FF 74AC74 were working to 160MHz and upper frequency limit for DR2H+ is determined with 74HC4066 goes to 72-78MHz. All about LP or BP filters you can read in additional articles published at this site and they are not subject of this article. All types are possible assembled at the same RX PCB layout. If you are not using any type of filters missing components replace with jumpers. See at picture how it looks like.
DR2H+ Single side PCB dimensions 143 x 77 mm

DR2H+ parts placement with gain position
DR2H++ specifications are:

8. Receiving range is going from 30 kHz to 72 MHz for DIL ICs version!!! With built in last modern technology components like 74LVC74 and 74LVC4066 are and with external LO to 110MHz!!
9. IIP3 32-35dBm and it depends from setting and used programs. MDS -116 to -122dBm also with 24 bit external USB SB card Audigy NX2
10. Receiver image rejection is from 65 -30 dB with hardware realization only
11. Sensitivity 0.18-0.25uV for 10 dB S/N ratio, max S/N ratio I measured was 70dB.
12. SFDR (Spurious free dynamic range) is 94-96 dB, this results are with signals spaced 5 kHz and more.
   Results are not changing very much if we spaced two signals to classical 20 kHz or more (with new modern SMT ICs 74LVC4066 SFRD is 98- 99dB).
13. RX 1 dB compression point is + 5dBm!!!
14. Receiver has built in 4 channel CMOS oscillator

DR2H++ Single side PCB size is 143 x 77 mm
DR2H++ parts placement with gain position

DR2H++ parts placement for 3 coils low-pass and external LO connection
DR2H++ Connection for internal overtone mode oscillator over 30 MHz and one kind of BP filter

DR2H++ Connection for block oscillator without input filter
To achieve max input receiving frequency it is necessary substitute DIL ICs with SMT 74LVC74 and 75LVC4066. It can be realized very simple with SMT adapters. SMT adapter for 74LVC40066 IC solder at top DR2H++ (DR2H+) side (add 10nF SMT for better HF RF decoupling). Solder with resistor leads through holes PCB to the DR2A++ PCB bottom side first. After first SMT adapter was soldered than solder SMT chip 74LVC4066. Vcc max = + 5V!!!!!!

SMT adapter single side PCB is size 11.4 x 20.7 mm for 74LVC74 (Vcc max is 3.6 V for Fin max 300 MHz) Vcc max = + 5V with adapter PCB we will enable work up to 110 MHz!!!!!! . In case that we use 74LVC4066 change values for resistors R19, 20, 21, 22 from 33Ohms to 82 Ohms.
Single side SMT adapter PCBs (for 74LVC4066 and 74LVC74 right) top view dimensions are 21 x 11.5 mm

Some excellent performances for both receivers aren’t without other side:

1. First and very big disadvantage is 2 times higher LO
2. Image rejection is changing through receiving bands. Given results are done for frequency 12 kHz from central frequency and with external sinusoidal +10dBm LO.
3. For external LO it is necessary input level around 1 Vp-p min for safe operation (for lower LO drive operations are not sure especially for higher LO frequencies)!!!Simple test for 74HC4066(74LVC4066) correct operation is when we measure with DMM (digital multi meter) Vcc/2 or 2.5 V +/-0.5 V at control pins 12, 13 and 5, 6 If it isn’t true we a problem with input LO level or input ICs 74AC74 or 74HC4066 (74LVC4066).
4. If we are using digital LO than it is very important that it has shape close to the 50-50% duty ratio to achieve similar results as with sinusoidal LO.

DR2H+ / DR2H++ adjustments are simple and done in two steps:

1. Adjust with universal instruments DMM (digital multi meter) that is resistance in feedback parallel connections potentiometer 500Ohms and 330Ohms = 150 Ohms.
2. Find some strong signal in the air 12 kHz away from zero or connect signal from signal generator to the input of DR2A++ and with 100Ohm potentiometer adjust the minimum unwanted image signal in some SDR program. Additional image rejection adjusts in SDR programs if this possibility exists function such as skew in Alberto I2PHD programs.

I wish you successful DR2H+ and DR2H++ realization and I apologize for some possible mistakes. I made great effort to make SDR projects and share them with all who are interesting for. Anyway send me your comments positive or negative, results or photos of your realization please.
DR2H++ prototype built by Jean-Michel TR8JH

VY 73/72 and GL in SDR homebrew Tasa YU1LM/QRP

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Software LINK for SDR radio receiving and transmitting

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