Monoband SDR HF S/H Sample and Hold Receiver with LO at working frequency - DR2C from 30 KHz to 50 MHz-Make it Simple as Possible with Outstanding performances

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Many HAMs all over the world built my SDR S/H receivers DR1, DR2, DR2A, DR1A…. you can see some photos on my sites and I can noticed that they are all satisfied with results . Simple constructions with cheap classic components working really very well. Also I find at INTERNET that some solutions from my receivers/transmitters are used in some new SDR projects.

I made local demonstrations of my SDR projects here in Belgrade. Presentation was for KKE club in YU1EXY club. Audience was very surprised with very good received demodulated signal quality, crisp and clear sound like HI-FI (high fidelity) not common for the most commercial RIGs. SDR possibilities such as adjustable selectivity, noise reduction, NB noise blanker; waterfall… was discovery for most of them. Local HAMs first excitements with new SDR techniques ware replaced with some disappointment because most HAMs like to tune LO (local oscillator) all over the working band and they are not satisfied with +/- 20 KHz with fixed LO. Also some easy obtainable XTAL quartz or OSC are not in very interesting parts of HF HAM bands. It is not easy build or it wasn't easy to build ever stabile LO at 120 MHz for 30 MHz or 56 MHz for 14 MHz. DDS LO is not easy to build for most builders also, a lot of reasons: hard to find IC-s, expensive and SMD components, needs for precise PCB for IC soldering…. Other solutions like PLLs are not so easy for realization also. In meanwhile I made some experiments how to simplify my simple SDR construction with even simpler and cheaper design. I decided to try new SDR design with some other IC and make SDR closer to HAM which like to try new technique with less problems cased with high LO frequencies. Result is HF SDR S/H receiver DR3X one LO or XTAL enable 3 bands harmonically related receiving.

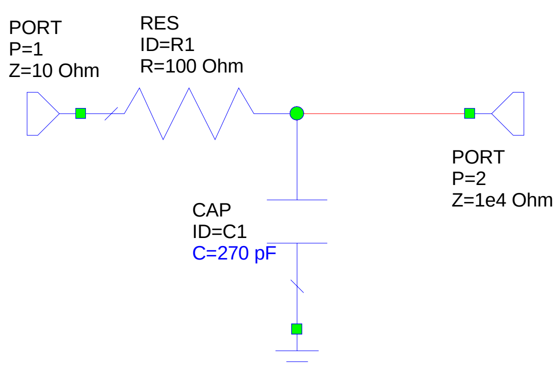
I also decided to try some not optimum technique obtaining I/Q 90 DEG branches for driving CMOS switches ref2 instead better technique with double D FF 74AC74 for max input frequency . Advantage of using 50/50 % duty cycle technique I explained in previously articles. Advantage is evident very much in my SDR transmission projects DT1, DT2 and DT2A. In receivers this 50/50 % ratio is not so important like for the transmission except for increasing max input frequencies with used hardware realization.

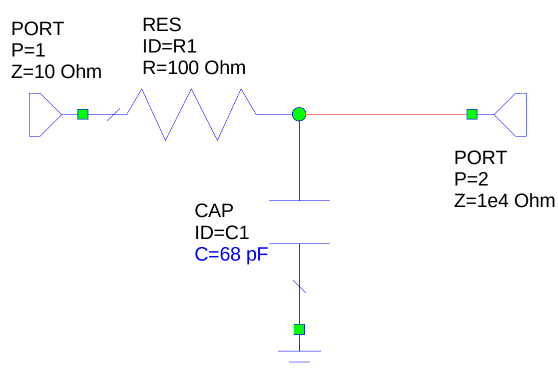
Here is a new one monoband HF SDR S/H receiver called DR2C with LO at receiving frequency from 30 KHz to 50 MHz. 90 DEG shift is obtaining with RC LP (low pass) network. What is very important for design it is gate output impedance which is driving RC networks is small as possible. At that way its output impedance influence to 90 deg phase shift is small as possible. Because of that I paralleled 3 inverters 74HC04 to decrease output impedance. It is important that is at output first inverter duty cycle close to optimum 50/50 % also. This is easy obtain able with clear sinusoidal drive signal with high amplitude 1 Vp-p or more for example. This solution is frequency depending design Exactly 90 deg shift is only at one frequency but for some practical used bandwidth it is OK. This mean that is possible satisfactory receive with relative good image rejection almost in all HAM bands to 50 MHz .Change inside most band is under 1 DEG. This is very important if you like to try SDR technology in commercial RIG as new IF . Design is also temperature sensitive .There is some change in 1 or 0 logical levels with bigger temperature change for CMOS ICs. In normal temperature range or room temperature work phase change with temperature change is very small. To reduce this problem little help is 10 K resistor at input of invertors.

Solution for phase shift with increasing R have big disadvantage for higher HF frequencies shift capacitor C became small and close to parasitic C inside IC invertors. In schematic I proposed some values for all HAM bands to 50-60 MHz which is close to the upper limit for IC 74 HC 4053 but it is possible other different components combination also. Components placement is done first for all 3 possibilities together XTAL quartz OSC, DIL OSC and external LO connection. Individual. XTAL quartz OSC is working to 30 MHz this schematics will not working on overtone quartz frequencies and frequencies over 30 MHz! For the receiving frequencies over 30 MHz LO source is possible DIL oscillator or some external oscillator working to 50 MHz with levels min 0 dBm.

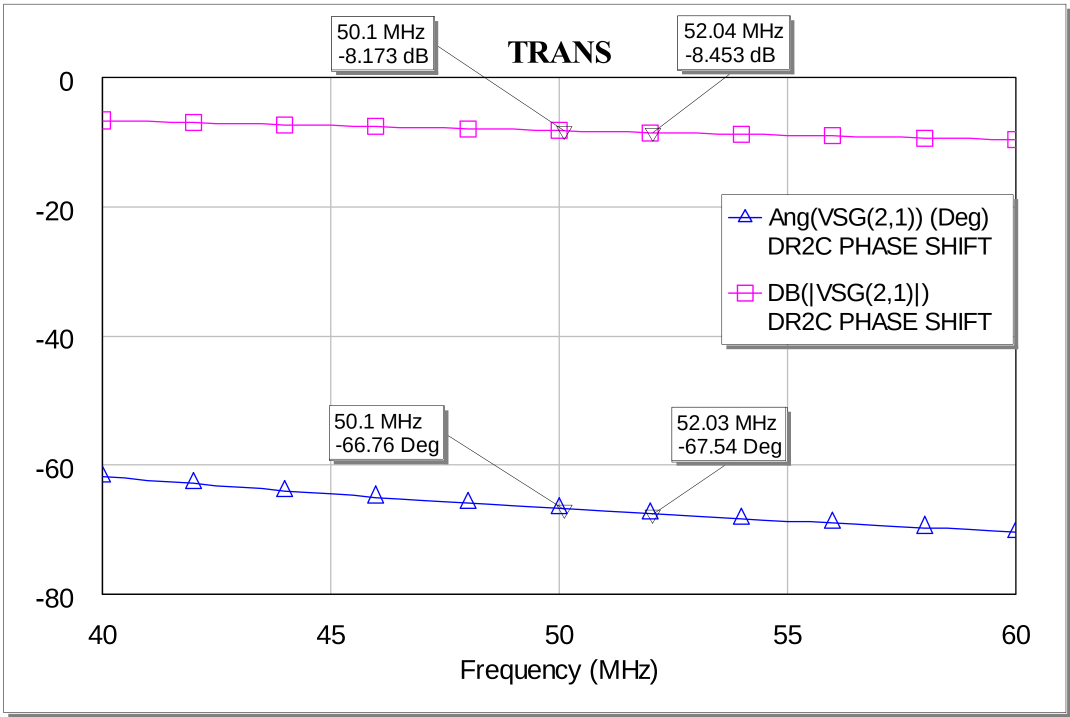
This design is ideal for build in inside some RX to obtain I/Q outputs for SDR sound card DSP processing. Carrier USB/LSB quartz can be easily move up 3-10 kHz with help C23. This mean that is LF IF in region 3-10 KHz that is enough to use I/Q with better success than ordinary AF sound card processing. Value for capacitor C23 is necessary to determine and obtain optimum max frequency shift and stabile oscillation at the same time.

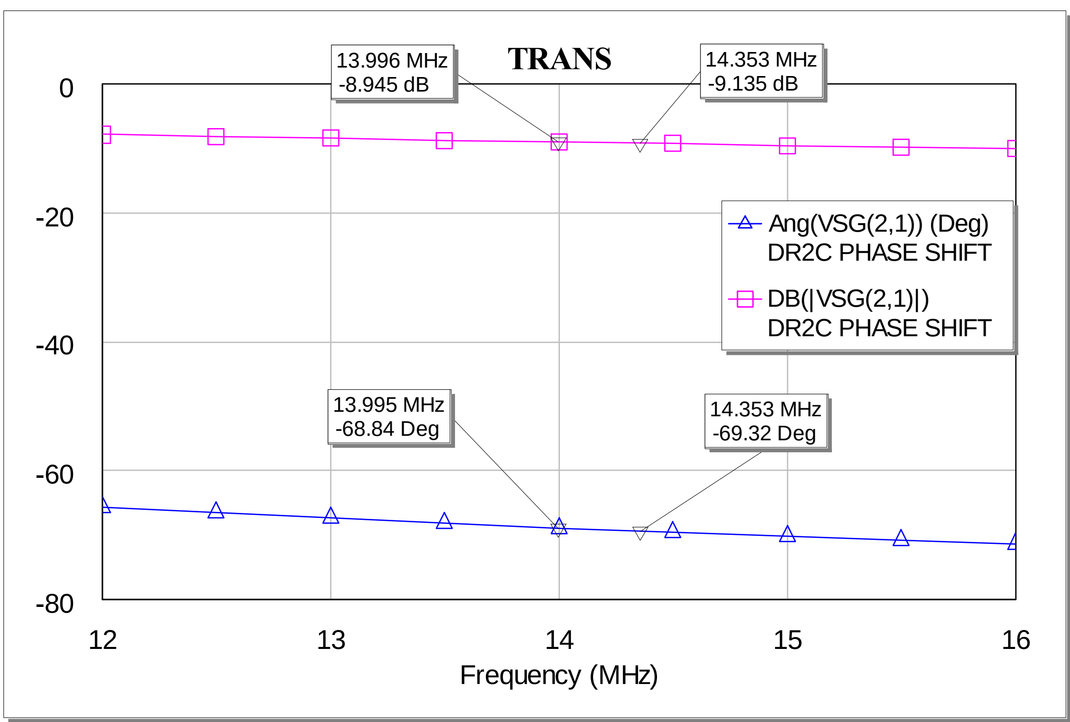
RC Shift network are not shifting 90 DEG initially but shift is around 66 DEG. Signal which is coming to the inverter gate is not sinusoidal wave signal but close to saw signal .We have a DC level for changing inverter levels from 1 to 0 or vice versa also. Together we obtain 90 DEG. See simulation curves are done for 14 MHz and 50 MHz bands.



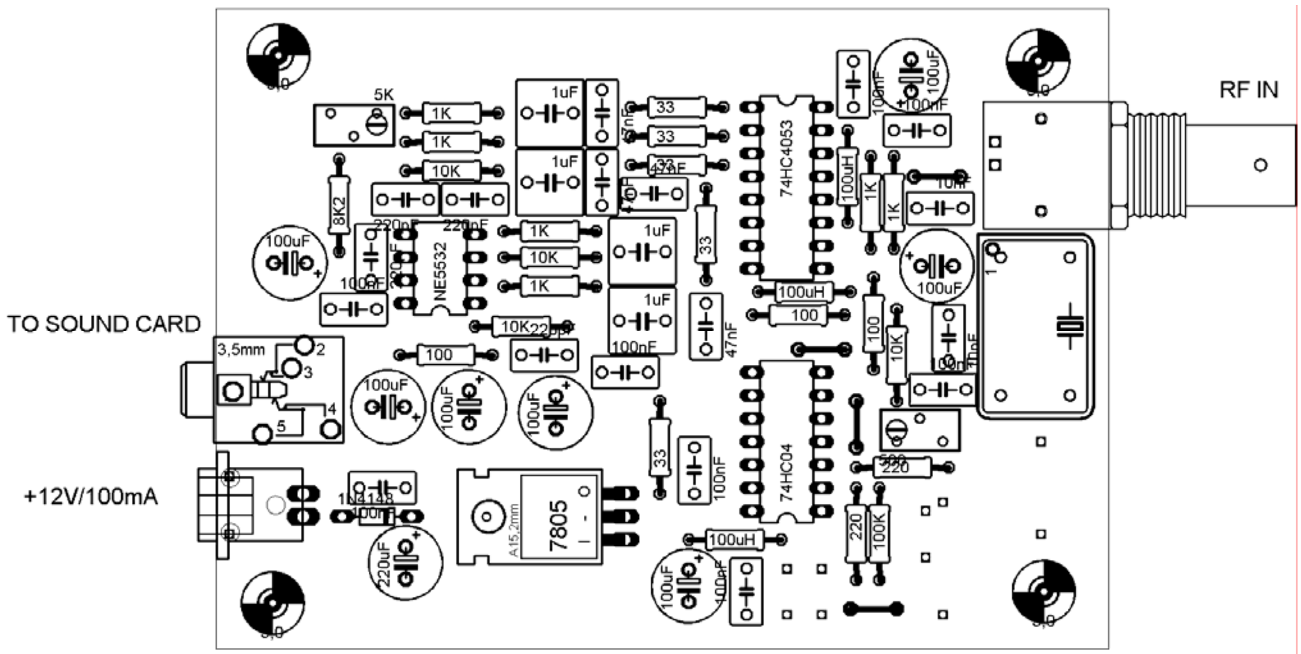


Values for phase sift network on 14 MHz and 50 MHz bands

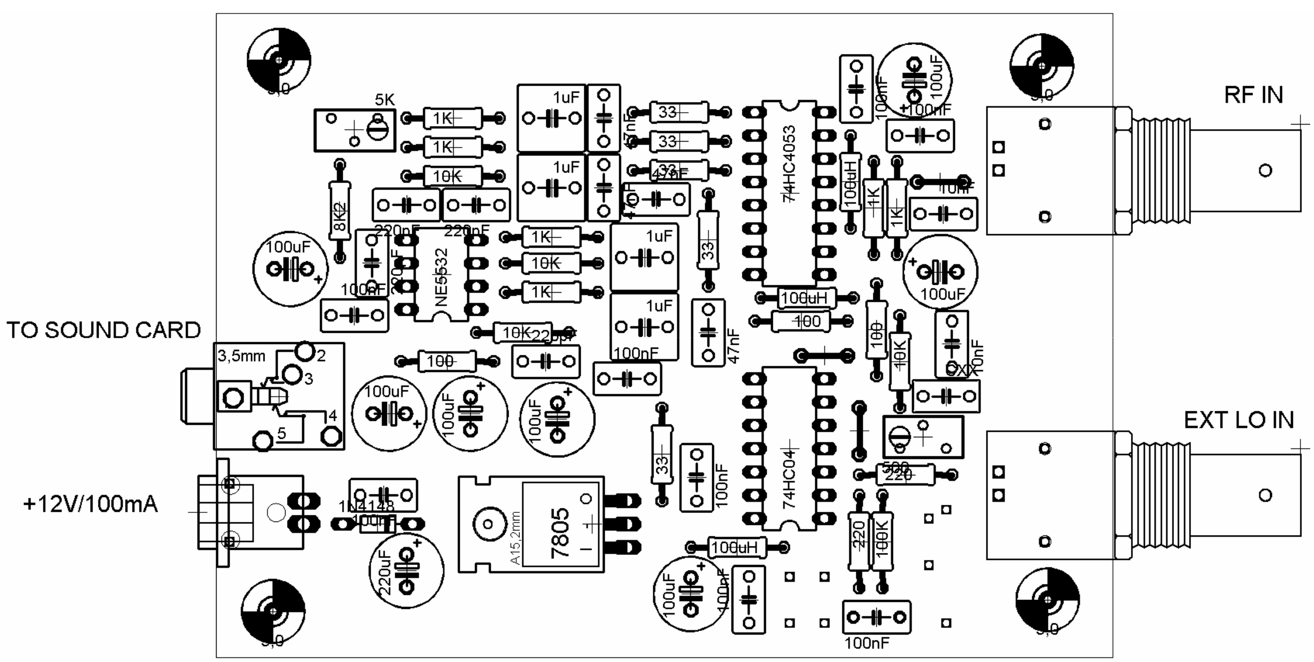




Phase shift simulation for both bands to notice in band phase change



Parts placement for DIL oscillator

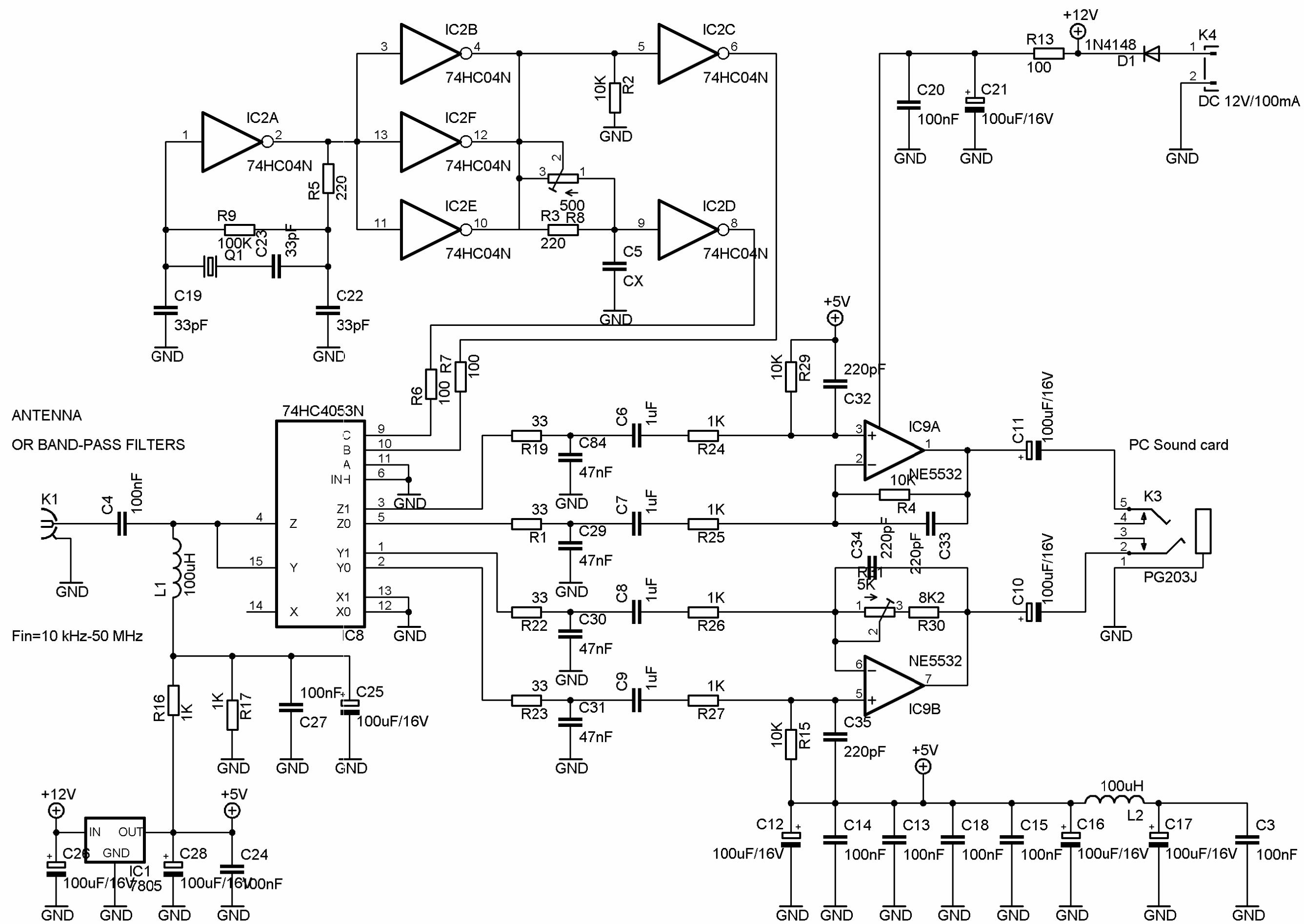


Parts placement for external oscillator

HF I/Q SDR Receiver DR2C - YU1LM/QRP

30 kHz-50 MHz

CX 1.8 MHz =2.2 nF CX 10.1 MHz =330 pF CX 24.9 MHz =150 pF
CX 3.5 MHz =1 nF CX 14 MHz =270 pF CX 28 MHz =100 pF
CX 7 MHz =560 pF CX 18.1 MHz =220 pF CX 50 MHz =68 pF



CONNECTION FOR INTERNAL OSCILLATOR

HF I/Q SDR Receiver DR2C - YU1LM/QRP

30 kHz-50 MHz

CX 1.8 MHz =2.2 nF	CX 10.1 MHz =330 pF	CX 24.9 MHz =150 pF
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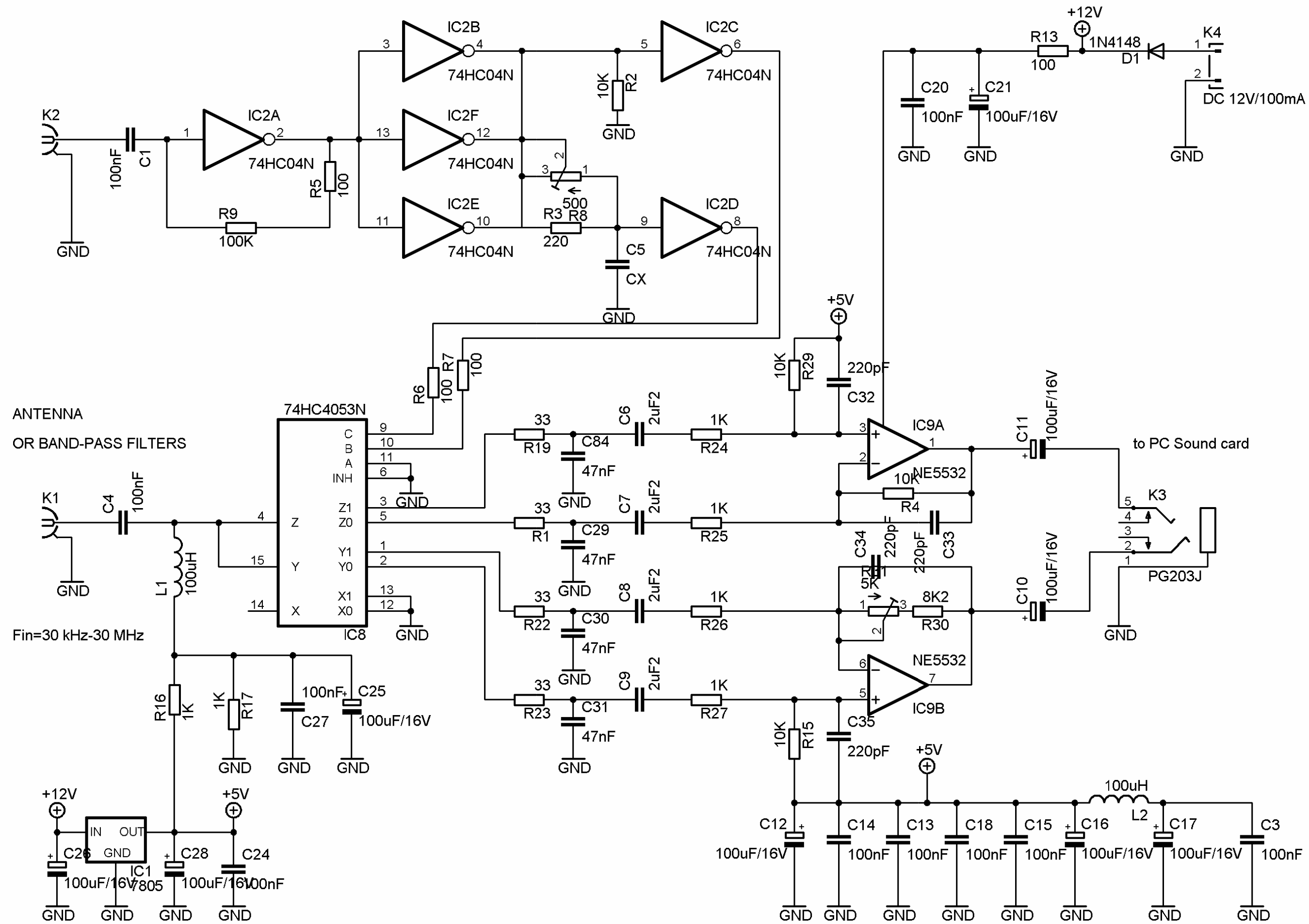
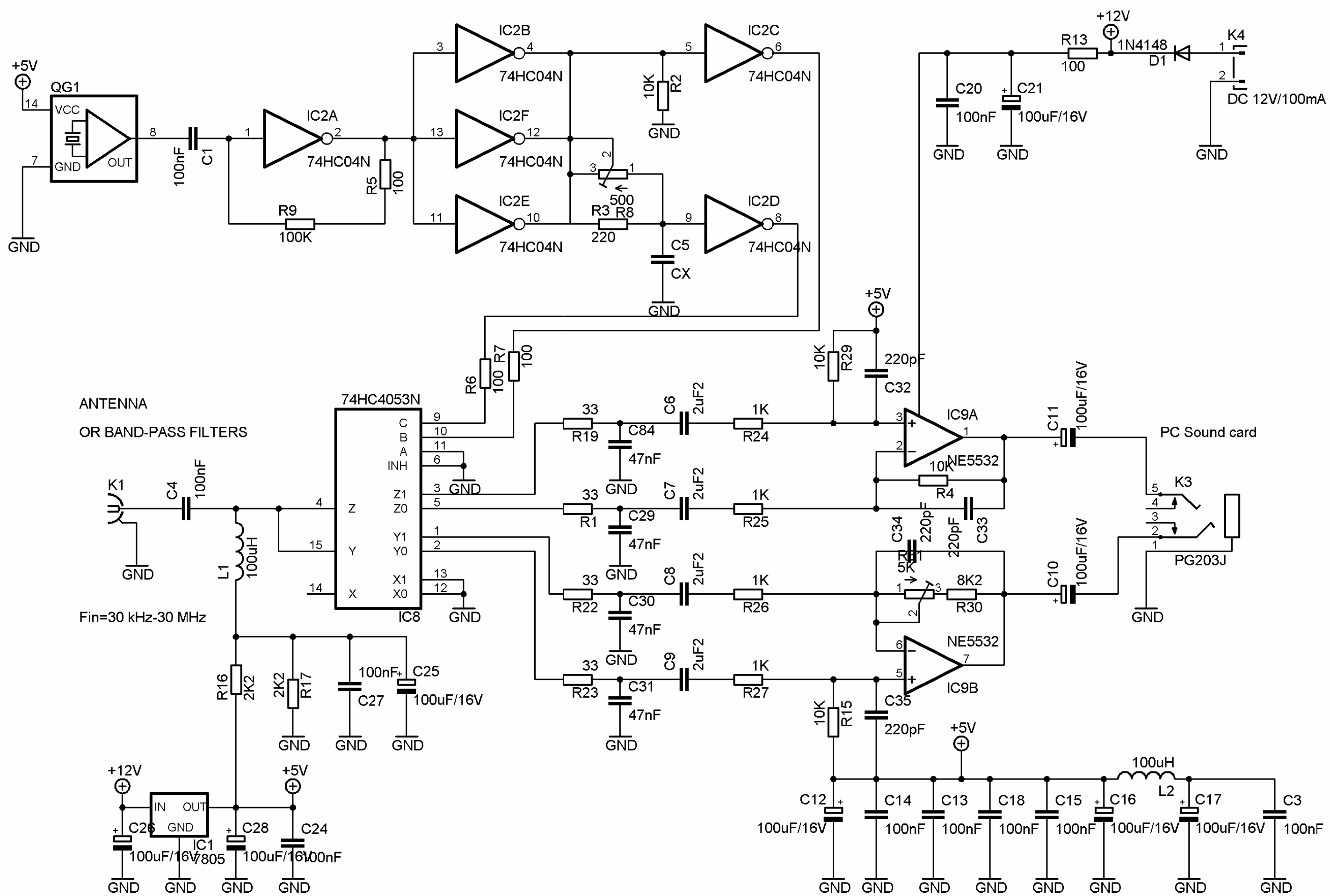


CONNECTION FOR EXTERNAL OSCILLATOR

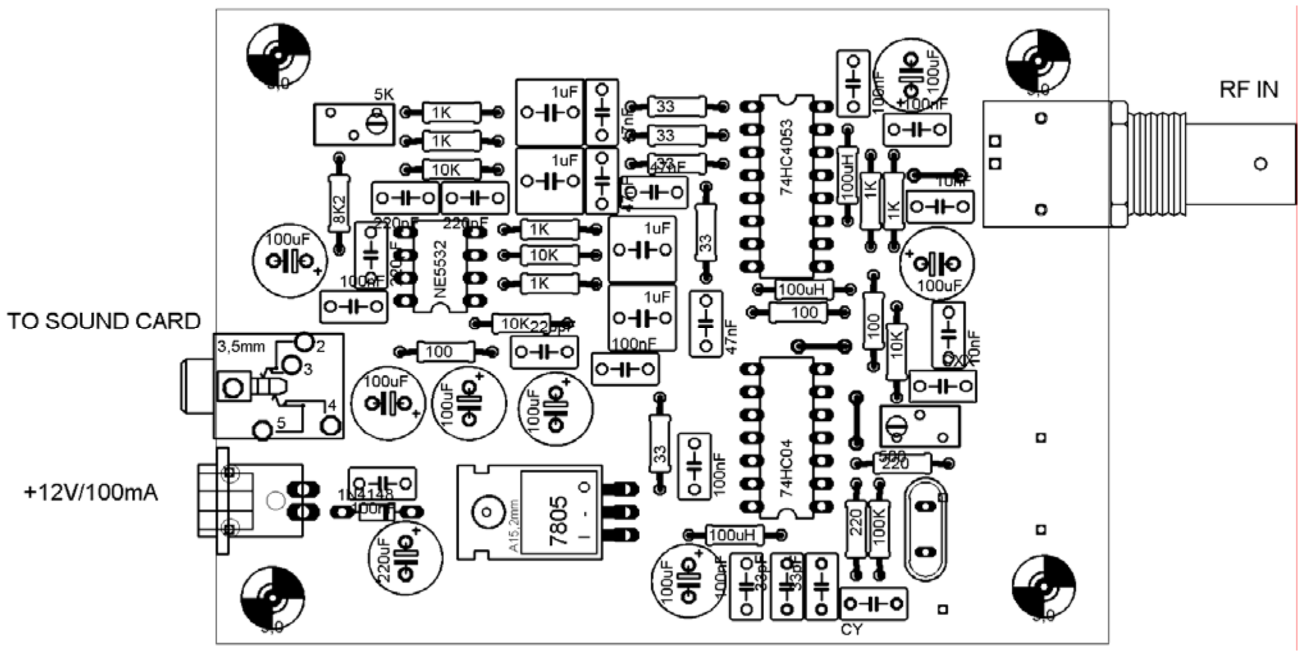
HF I/Q SDR Receiver DR2C - YU1LM/QRP

30 kHz-50 MHz

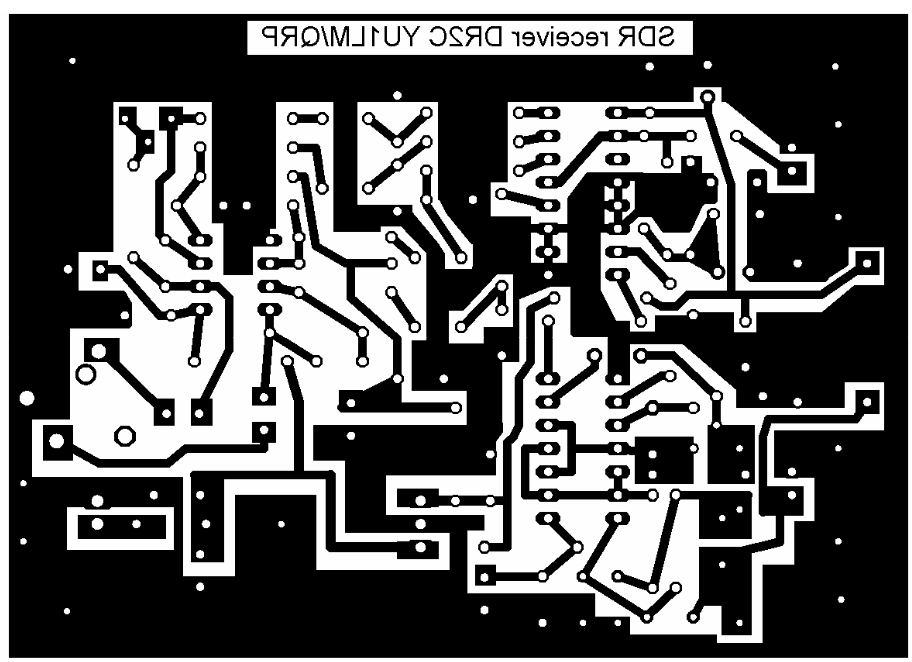
CX 1.8 MHz =2.2 nF CX 10.1 MHz =330 pF CX 24.9 MHz =150 pF
CX 3.5 MHz =1 nF CX 14 MHz =270 pF CX 28 MHz =100 pF
CX 7 MHz =560 pF CX 18.1 MHz =220 pF CX 50 MHz =68 pF



CONNECTION FOR DIL OSCILLATOR



Parts placement for internal oscillator, PCB size 97 x 70 mm



Measuring results I obtained with DR2C:

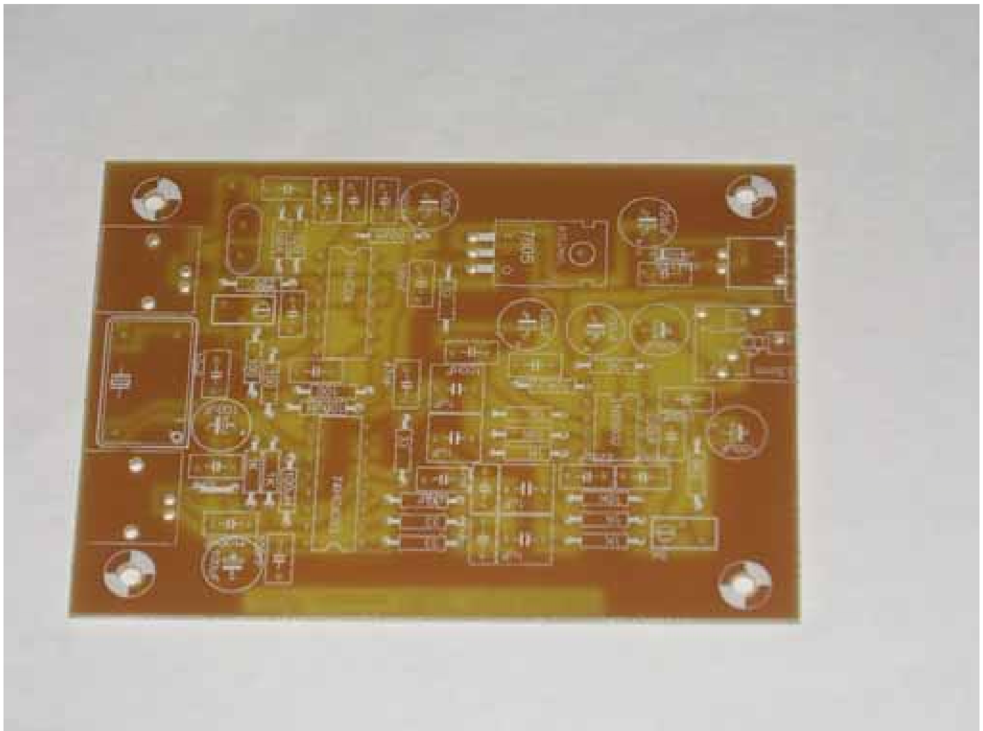
1. Receiving range from 30 kHz to 50 MHz (with Q unit oscillator it is limited to the 30 MHz)
2. IIP3 27-29 dBm it depends from setting and used programs (all done with 16 bit sound cards). Max measured IIP3 with only 6 dB AF gain was 33 dBm but with reduced sensitivity
3. MDS -102-105 dBm also with 16 bit SB card
4. Image rejection is possible adjust to 60-70 dB at single frequency.
5. Sensitivity is 3-5 uV for 10 dB S/N ratio, max S/N ratio I measured was 70 dB. This sensitivity is more than enough for frequency near to 20 MHz with adequate antenna system, for higher frequency it is recommend increasing AF gain or putting some RF preamplifier in front of DR1 to lower F (noise figure) of receiver.
6. SFDR (Spurious free dynamic range) is 86-92 dB, this results are with signals spaced 5 kHz and more. Results are not changing very much if we spaced two signals to classical 20 kHz or more. All measurements are done by use HP8662 signal generators and HP 70000 series spectrum analyzer.

Some excellent performances with 3 IC are not without other side:

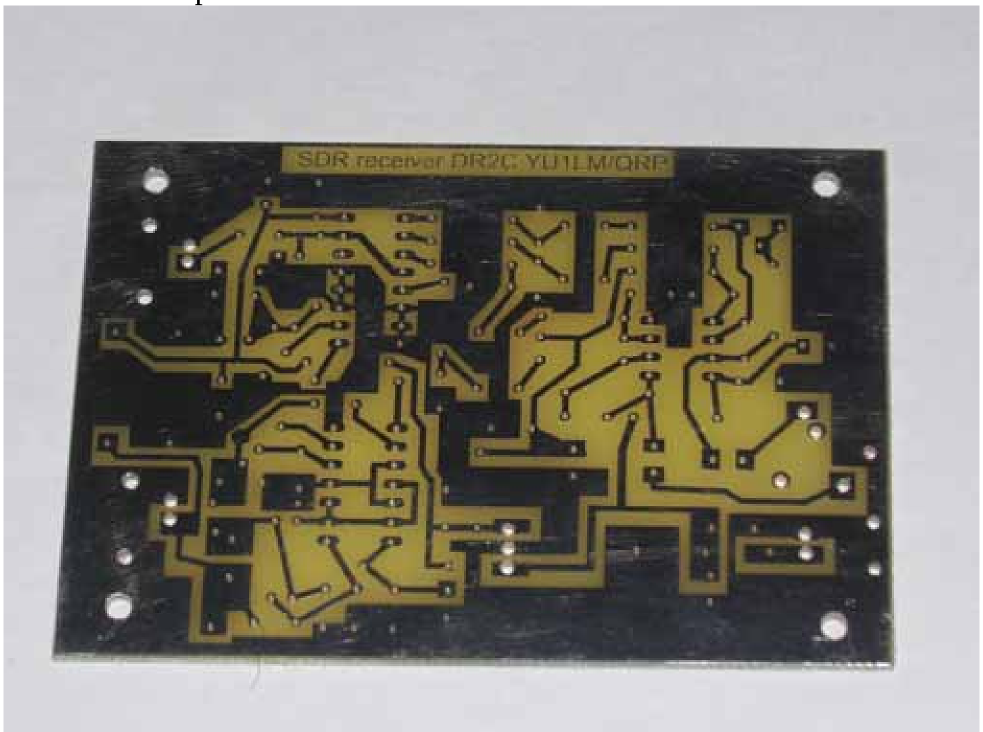
1. First and very big disadvantage is single band receiving
2. Image rejection is changing through receiving band.

DR2C adjustments are simple and done in two steps:

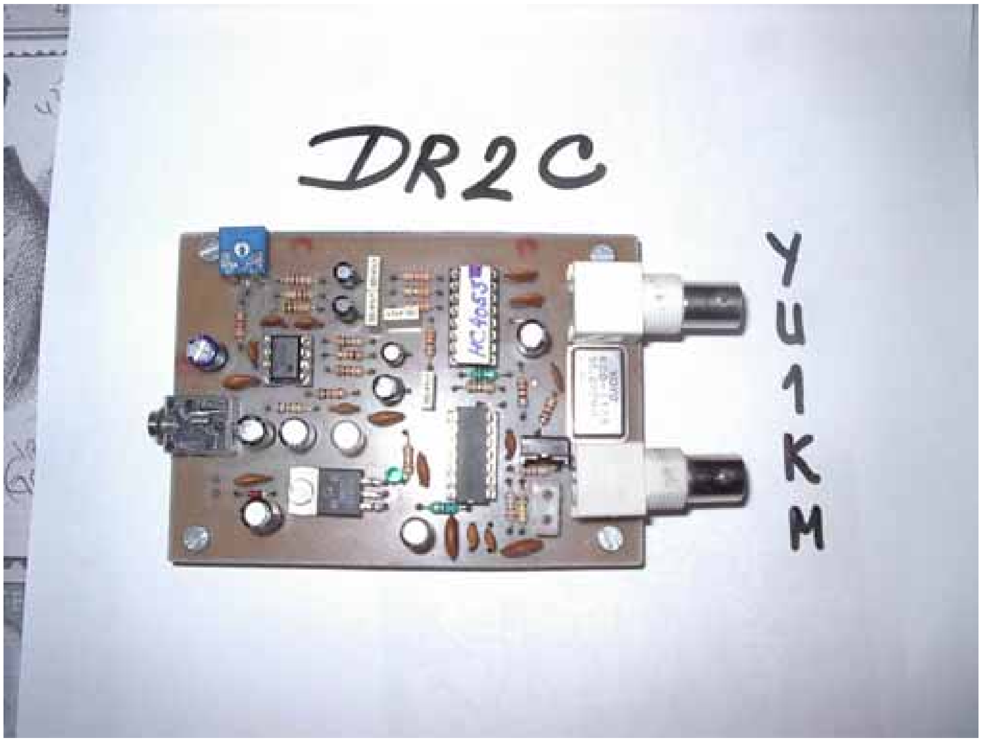
1. Adjust with DMM (digital multimeter) that is resistance in feedback potentiometer 5k +8K2 = 10 K.
2. Find some strong signal in the air 12 kHz away from zero or put signal from signal generator to the input of DR2C in middle band and with 500 Ohm potentiometer adjust min unwanted image in used SDR program. Next step is with 5 Kohm potentiometer adjust new minimum of unwanted image signal. This procedure repeats few times to obtain optimum Additional image rejection adjust in SDR programs if this possibility exist (skew option in Alberto I2PHD programs).



DR2C PCB top view



DR2C PCB bottom view



First DR2C version built by Miki YU1KM

I wish you successful DR2C realization and I apologize for some possible mistakes. I made great effort to make SDR projects and share them with all who are interesting for. Anyway send me your comments positive or negative, results or photos of your realization please.

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References:

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2. ***http://forum.cqham.ru/viewforum.php ?f=28***
3. ***Skidan@mail.ints.net T03DSP UR3IQO http://users.ints.net/skidan/T03DSP***
4. ***http://www.nitehawk.com/sm5bsz Leif LINARD***
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http://hem.passagen.se/communication/dds.html

7. ***Recent Advances in Shortwave Receiver Design Dr. Ulrich Rohde QST Nov 1992 page 53***
6. ***RF Design 6/1995***

Software LINK for SDR radio receiving and transmitting

1. ***http://digilander.libero.it/i2phd/ SDRadio software ver 0.99***

   www.qsl.net/i2phd Alberto I2PHDhttp://gpsdo.i2phd.com/
2. ***ik2czl@weaksignals.com <ik2czl@weaksignals.com>ik2czl@weaksignals.com <ik2czl@weaksignals.com>Vittorio***
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7. ***http://www.nitehawk.com/sm5bsz Leif LINARD***
8. ***http://www.flex-radio.com SDR1000 Gerald AC5OG***
9. ***dl6iak.ba-karlsruhe.de***